REMARKS

Initial notes

Applicant has reviewed the Examiner's latest office action in its entirety, and has amended the claims and provided arguments herein as to why the pending claims are allowable. Applicant is eager to obtain the allowance of this patent application. While Applicant firmly believes that the pending claims are allowable, he is very much willing to consider additional claim language that would satisfy the Examiner. **Therefore, if the Examiner believes that certain claim language added to the claims would render the present patent application allowable, he is very much encouraged to contact Applicant's representative, Mike Dryja, at the phone number listed below.**

Objections to the claims

Claims 16 and 17 have been objected to because of a typographical/grammatical error in claim 16, in which the phrase "a predetermined *value the* current operation" is recited. Applicant has amended claim 16 to correct this error, so that this phrase now correctly reads "a predetermined *value of the* current operation."

Claim 9 has been objected to because it fails to further limit the subject matter of a previous claim. While Applicant does not necessarily agree with the Examiner, to further the patent application to allowance, he has cancelled claim 9 without prejudice.

Claim rejections under 35 USC 112

Claims 8-10 have been rejected under 35 USC 112, second paragraph, as being indefinite. In particular, claim 8, from which claims 9 and 10 ultimately depend, is believed by the Examiner to have two bases of indefiniteness. First, the Examiner has stated that there are four claimed inputs to the multiplexer, whereas the figures and the specification recite just three inputs. These

four claimed inputs are stated as: the selected fields of the first register; the comparator output; the predetermined responsive value; and, the alternative responsive value.

Applicant has reviewed claim 8 in this respect, and believes that any potential indefiniteness lies in the fact that it is not clear that the first register storing the selected fields also stores the alternative responsive output. Thus, there are indeed three inputs to the multiplexer: the first register, which provides the selected fields and the alternative responsive output; the transaction lookup table, which provides the predetermined responsive output; and, the comparator. Therefore, Applicant has amended claim 8 to make it clear that the multiplexer "receives the alternative responsive output as input from the first register."

Support for this amendment to claim 8 is found at least in the patent application as originally filed in two places. First, it is stated on page 10, lines 5-6 that "the transaction response register (TRR) 54 provides an alternative response." Second, it is stated on page 11, lines 15-20, that:

> TRR 54 is comprised of four fields, memory command 80, input/output (IO) command 81, attribute field 82, and target field 83. If a particular transaction is identified as a transaction requiring an alternate response, that is, different from the response originally programmed in transaction look-up table 56 *TRR 54 provides the new response. The desired redirected response is loaded in TRR 54* to be communicated to input 79 at Mux 60 to present the corrected output 76.

Therefore, it is clear from the patent application as filed that the TRR 54 stores selected fields, namely the fields 80, 81, 82, and 83, and that the TRR 54 inputs the fields into the mux 60 at the input 79, as evidenced in FIG. 1B in particular. Furthermore, it is clear from the patent application as filed that the TRR 54 receives the alternative responsive output from the TRR 54, in that the TRR 54 has loaded thereinto the alternative responsive output that is also communicate to the input 79 of the mux 60.

As a result, Applicant believes that claim 8 now satisfies 35 USC 112 in this regard. However, if the Examiner believes that this claim is still unclear, Applicant is very much amenable to considering proposed claim language that would render this claim definite to the satisfaction of

the Examiner. To this end, the Examiner is very much encouraged to contact Applicant's representative, Mike Dryja, at the phone number listed below, with such suggested claim language.

Second, the Examiner has also stated that claim 8's recitation of "outputting said new transaction results to a register" requires further clarification as to what the "new transaction" referred to is. Applicant has amended claim 8 so that it now recites "outputting corrected transaction results," where these results are "one of the predetermined responsive value and the alternative responsive output." That is, the correct transaction results outputted by claim 8 (formerly the "new transaction results") are either the predetermined responsive value or the alternative responsive output.

As a result, Applicant also believes that claim 8 now satisfies 35 USC 112 in this regard, too. Again, however, if the Examiner believes that this claim is still unclear, Applicant is very much amenable to considering proposed claim language that would render this claim definite to the satisfaction of the Examiner. To this end, the Examiner is very much encourage to contact Applicant's representative, Mike Dryja, at the phone number listed below, with such suggested claim language.

Claim rejections under 35 USC 103 as to claims 1-5, 8-9, 11-12, and 14-18

Claims 1-5, 8-9, 11-12, and 14-18 have been rejected under 35 USC 103(a) as being unpatentable over Johnson (5,796,972) in view of Jim Handy, The Cache Memory Book, 2nd edition, which is hereinafter referred to as Handy. Applicant respectfully traverses this rejection, insofar as Handy is not properly combined with Johnson under 35 USC 103(a). This is now discussed in detail.

The Examiner has stated that Johnson teaches all aspects of the claimed invention, except that it fails to teach a comparator as recited in the claims. However, the Examiner notes that

Handy teaches CAM memories, which can be considered a comparator. Therefore, the Examiner has combined Handy with Johnson to yield all the claim limitations of the claimed invention.

Applicant does not necessarily agree with the Examiner in this respect, but very respectfully submits instead that Handy is not properly combined with Johnson for two separate and independent reasons. First, there is no reason, suggestion, or motivation to modify Johnson as per Handy as recited by the Examiner. Second, Handy in fact teaches away from combination with Johnson. Each of these separate and independent reasons is now discussed in detail.

First reason: No suggestion or motivation to modify Johnson as per Handy

Applicant first submits that there is no suggestion or motivation to modify Johnson to employ the CAM memories of Handy. The Examiner's stated suggestion or motivation to modify Johnson per Handy is recited in the most recent office action as follows:

> It would have been obvious to one of ordinary skill in the art to replace the indexable memory of Johnson with the CAM memory of Handy since CAM memories are widely known in the art as alternatives to indexable memories and allows any entry to point to any location and have parallel access to each comparator so there is no hindrance on performance. Furthermore, a CAM memory would logically perform the same operation the indexable memory is performing. An identifying data portion is input to the memory, and the associated data is retrieved, in both the indexable memory and the CAM memory.

(P. 7, para. 17) Applicant believes that this stated suggestion or motivation of modify Johnson per Handy has two parts. The first part is that it would have been obvious to modify Johnson to employ the CAM memories of Handy because "CAM memories are widely known in the art as alternative to indexable memories." However, the MPEP is clear that the "fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish *prima facie* obviousness." (MPEP 2143.01.IV.)

Indeed, the language employed in the case law as to this first part is identical in substance to what the Examiner has stated. That is, the MPEP notes that "[a] statement that modifications of the prior art to meet the claimed invention would have 'well within the ordinary skill of the art

at the time claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prime facie* case of obviousness without some objective reason to combine the teachings of the references." (Id.) In this respect, the MPEP quotes Ex parte Levengood, 28 USPQ2d 1300 (BPAI 1993). Now, compare this recitation of the MPEP, that modifications of the prior art are improper where the prior art is only "well within the ordinary skill of the art" to the Examiner's recitation that "CAM memories are widely known in the art as alternatives to indexable memories." Applicant submits that in substance the Examiner is stating in this first part of his stated suggestion or motivation to modify Johnson per Handy is that it is well within the ordinary skill of the art to replace indexable memories with CAM memories. However, per the MPEP and case law, just because it is known that the former are replaceable with the latter does not rise to the level that there is a suggestion or motivation to modify Johnson to use the CAM memories of Handy.

The second part of the Examiner's stated suggestion or motivation to modify Johnson per Handy is that "CAM memories . . . allow[] any entry to point to any location and have parallel access to each comparator *so there is no hindrance on performance*" and that "a CAM memory would logically perform the same operation the indexable memory is performing." Applicant submits that in substance the Examiner is saying here that you can use the CAM memories of Handy instead of the indexable memories of Johnson because: 1) they logically perform the same thing; and, 2) there is no hindrance on performance in doing so, since CAM memories allow any entry to point to any location and have parallel access. However, the MPEP is also clear that the "fact that references *can* be combined or modified is not sufficient to establish *prima facie* obviousness." (MPEP 2143.01.III.)

More specifically, case law is relied upon by the MPEP as supporting that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." In this respect, the MPEP

relies upon In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Now, the Examiner is saying that CAM memories logically perform the same way as indexable memories, and that replacing the indexable memories of Johnson with the CAM memories of Handy results in no hindrance on performance. However, both of these things go to the fact that Johnson "*can* be combined with Handy" – and most significantly, neither "suggests the desirability of the combination." That is, that CAM memories logically perform like indexable memories does not suggest the desirability of using CAM memories instead of indexable memories. Furthermore, that using CAM memories instead of indexable memories does not result in any performance hindrance does not suggest the desirability of using CAM memories (i.e., why they should be used) instead of indexable memories.

Therefore, there is no reason or motivation to modify Johnson to use the CAM memories of Handy instead of the indexable memories of Johnson. In the first part of his reasoning, the Examiner states that "CAM memories are widely known in the art as alternatives to indexable memories." However, the fact that the claimed invention is within the capabilities of one of ordinary skill within the art is not sufficient by itself to establish *prima facie* obviousness. In the second part of his reasoning, the Examiner states that CAM memories logically perform like indexable memories do, and that there is no hindrance in performance in using CAM memories instead of indexable memories. However, neither of these suggests the desirability of using CAM memories instead of indexable memories, such that the mere fact that these two references can be combined does not render the resultant combination obvious, since the prior art does not also suggest the desirability of this combination. For these reasons alone, there is no *prima facie* obviousness of the claimed invention.

Second reason: Handy teaches away from combination with Johnson

Applicant second submits that Handy teaches away from combination with Johnson. That is, Handy provides a reason not to be combined with Johnson. As such, Handy provides a disincentive to use its CAM memories in place of the indexable memories of Johnson.

Before getting into the specifics of Handy's teaching away from combination with Johnson, the case law that Applicant relies upon in this respect is noted. The MPEP notes that "[a] prior art reference must be considered in its entirety, i.e., as a whole, *including portions that lead away from the claimed invention*." (MPEP sec. 2141.02.VI.) In this respect, the MPEP relies upon W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983). Thus, Handy's reason as to why CAM memories should not be used must be considered, insofar as Handy must be considered in its entirety.

Now, Applicant notes that Handy recites the following:

> The reader might ask "Why aren't CAMs widely available?" The simple reason is that much simpler schemes perform nearly as well as the CAM approach, yet can be constructed from standard static RAMs and allow the use of less expensive cache data RAMs. . . . Cache designers are not ready to pay as much for CAMs as CAMs would have to cost to attract the interest of semiconductor manufacturers. The author knows of only two kinds of CAMs available on the market today.

(P. 15, last paragraph) Thus, there are two big disincentives and demotivations to modify Johnson in view of Handy. First, Handy's CAM memories are more complicated to use than other, simpler schemes (like Johnson's indexable memories), and these other, simpler schemes perform nearly as well. Therefore, because Johnson's cache memory scheme performs just fine the way it is recited, there is no motivation to modify it to instead use CAM memories, where doing so would be much more complicated than simply using indexable memories as recited in Johnson, with little performance benefit at best. For this reason alone, Handy teaches away from modification of Johnson per Handy.

[Indeed, Applicant submits that insofar as there are "only two kinds of CAMs available on the market today," attempting to use the CAM memories of Handy as a replacement for the indexable memories of Johnson would require a substantial reconstruction and redesign of the scheme taught in Johnson. That is, where Handy admits in substance that CAM memories are much more complex – insofar as Handy states that other types of memories are much simpler than CAM memories – and where there are only two kinds of CAMs available on the market today, Applicant submits that the Examiner cannot presume that the indexable memories of Johnson could be easily substituted by those of ordinary skill within the art by the CAM memories of Handy. Where a "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in [the primary reference]," "the teachings of the references are not sufficient to render the claims *prima facie* obvious." (MPEP 2143.01.VI., reciting In re Ratti, 270 F.2d 810, 813, 123 USPQ 349, 352 (CCPA 1959)) Indeed, since there are only two kinds of CAMs available on the market today, Johnson's cache memory scheme would have to be redesigned and reconstructed to use one of these two types of CAMs! For this reason alone, too, Handy teaches away from modification of Johnson per Handy.]

The second big disincentive and demotivation to modify Johnson in view of Handy is that they cost too much. That is, "[c]ache designers are not ready to pay as much for CAMs as CAMS would have to cost to attract the interest of semiconductor manufacturers," as particularly stated by Handy. Therefore, because Johnson's cache memory scheme performs just fine the way it is recited, there is no motivation to modify it to instead use CAM memories, where doing so would be more expensive, as admitted by Handy and which is also supported by the fact that there are only two kinds of CAMs available on the market today, and where little performance benefit at best would result. For this reason alone as well, Handy teaches away from modification of Johnson per Handy.

Final thoughts on the prima facie *combinability of Johnson and Handy*

At the end of the day, to modify Johnson per Handy would: (1) be much more expensive; (2) be much more complicated, and (3) likely require substantial reconstruction and redesign of Johnson, as recited above. All of these are reasons, motivations, and suggestions *not* to modify Johnson to use the CAM memories of Handy. On the flip side, as has also been recited above, the Examiner has not identified a single advantage that would result from using CAM memories in Johnson, instead saying that there would be no hindrance in performance, and that logical operation would remain the same. Therefore, there is nearly no upside in modifying Johnson per Handy. Thus, just because Johnson *could* be modified per Handy, does not make it *obvious* to do so – and indeed, Handy itself provides reasons why you would not want to do so! For all of these separate and independent reasons, then, Johnson is not properly combined with Handy.

Claim rejections under 35 USC 103 as to claims 7, 10, and 13

Claims 7, 10, and 13 have been rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Handy, and further in view of "The PowerPC Architecture: A specification for a new family of RISC processors," which is hereinafter referred to as PowerPC. Applicant respectfully traverses this rejection. Insofar as Handy is not properly combined with Johnson under 35 USC 103(a), as has been recited in depth above, claims 7, 10, and 13 are patentable under 35 USC 103(a) over Johnson in view of Handy, and further in view of PowerPC.

Claim rejections under 35 USC 103(a) as to claim 19

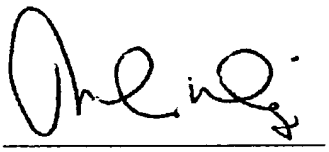
Claim 19 has been rejected under 35 USC 103(a) as being unpatentable over Johnson in view of Handy, and further in view of IBM Technical Disclosure Bulletin, vol. 37, no. 03, which is hereinafter referred to as IBM. Applicant respectfully traverses this rejection. Insofar as Handy is not properly combined with Johnson under 35 USC 103(a), as has been recited in depth above,

claim 19 is patentable under 35 USC 103(a) over Johnson in view of Handy, and further in view of IBM.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney so that such issues may be resolved as expeditiously as possible. For these reasons, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



March 13, 2006
Date

Michael A. Dryja, Reg. No. 39,662
Attorney/Agent for Applicant(s)

Law Offices of Michael Dryja
704 228th Ave NE #694
Sammamish, WA 98074
tel: 425-427-5094

fax: 206-374-2819